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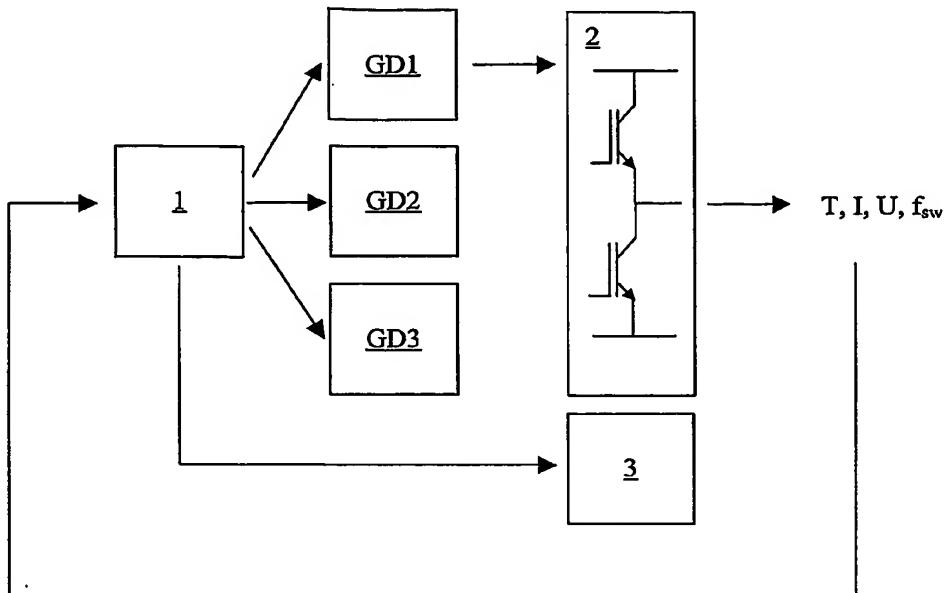
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(54) Title: **METHOD AND ARRANGEMENT IN INVERTER**



(57) Abstract: A method and arrangement in connection with an inverter that comprises several power semiconductor components and a control apparatus arranged to control them, the control apparatus being arranged to control the power semiconductor components in response to a control quantity to generate an output voltage. The method comprises the steps of determining the change of the temperature or a quantity affecting the temperature of one or more power semiconductor components, and controlling with the control apparatus the power semiconductor components in response to both the control quantity to generate an output voltage and the change rate of the temperature or quantity affecting the temperature of the power semiconductor components to reduce the temperature change and the change rate.

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**Declarations under Rule 4.17:**

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE,*

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